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S-2609

M. Sc. (Physics) (Sem. I) Examination

March / April – 2011

Paper - 414 : General Electronics

Time : **3** Hours] [Total Marks : **70**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **M. SC. (PHYSICS) (SEM. 1)**

Name of the Subject :

☛ **414 : GENERAL ELECTRONICS**

☛ Subject Code No. : **2 6 0 9** ☛ Section No. (1, 2,.....) : **NIL**

Seat No. :

Student's Signature

(2) This question paper includes five main questions each of which is with three sub-question (a), (b) and (c)

(3) Answer any Two sub-questions from each main question.

(4) Assume data if require.

(5) Symbols used have their usual meaning.

1 (a) What is the need of biasing ? With the help of the circuit diagram, derive the expression of biasing resistor R_b for the fixed biasing circuit of Bipolar Junction Transistor. **7**

(b) For the self biasing circuit of BJT, show mathematically that the slope of the load line is $(R_C + R_E)$. **7**

(c) Explain construction and working of an FET and define its (i) r_d (ii) g_m and (iii) μ parameters. **7**

2 (a) Draw the block diagram of an operational amplifier. With circuit diagram and formula, explain how a constant tail current attachment in the differential circuit enhances the CMRR. **7**

(b) Derive exact gain equation for an operational amplifier in inverting mode with negative feedback. **7**

(c) Using operational amplifier in non-inverting mode, design a circuit that performs the addition of its three input values V_a, V_b and V_c. **7**

3 (a) With suitable examples explain simplification method of four variables Boolean expression using K-map. 7

(b) Simplify following using Boolean relations and implement with basic logic gates : 7

(i) $Y = \overline{(B + A) \cdot A}$

(ii) $Y = \overline{\left(P + Q \cdot \overline{P}\right)}$

(c) What is the difference between full-subtractor and half-subtractor ? Design a full-subtractor circuit using logic gates. 7

4 (a) What is the difference between de-multiplexer and a decoder ? With circuit diagram and truth table, explain working of 1-line to 8-line de-multiplexer. 7

(b) Using basic logic gates design a 4-bit parity checker circuit. Explain its operation giving example. 7

(c) A diode matrix ROM circuit has 4-switches S_1, S_2, S_3 and S_4 connected at the input of the circuit. If the circuit is expected to give output as per the following table, design diode matrix ROM circuit. 7

Switch pressed	**output word**
S_1	001100
S_2	111111
S_3	101010
S_4	000001

5 (a) Design clocked R-S flip-flop using only NAND gates and explain its operation with truth table. 7

(b) Using suitable flip-flops, design 3-bit ripple down-counter and explain its working with table and waveforms. 7

(c) Design Mod-5 counter and draw its table and waveform. 7
